JOURNAL OF MATERIALS SCIENCE 15 (1980) 1124–1130

Role of a polysilicon layer in the reduction of lattice defects associated with phosphorus predeposition in silicon*

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This paper reports the analysis of lattice defects induced in silicon by phosphorus predeposition carried out at 920, 1000 and 1100° C through a polycrystalline silicon layer. The corresponding results obtained on bare wafers are also represented for comparison.

From transmission electron microscopy it was found that the precipitation of phosphorus, when it occurs, is confined within the polysilicon film, keeping the substrate free from this type of defect, even for very long predeposition times. In addition, X-ray topography showed that extrinsic stacking faults and dislocations were absent, although these are commonly observed when the doping process is performed under the same conditions on a bare single crystal.

This behaviour suggests that the polysilicon layer acts as a sink for the excess interstitials induced by the in-going phosphorus atoms. The resulting improvement of lattice perfection should allow fabrication of devices with better electrical performances.

1. Introduction

During the phosphorus predeposition in silicon single crystals point defects are generated, which induce marked modifications in the shape of the doping profiles (e.g. a plateau near the surface and a high diffusivity tail in the low concentration region) [1–3]. These defects are also responsible for the formation of both extrinsic stacking faults and dislocations [4, 5].

In addition, in the conditions typical of the planar technology, the phosphorus concentration in the region near the surface of the specimen exceeds the solubility limit during the predeposition process; this gives rise to the formation of rod-like SiP precipitates in the silicon matrix [6, 7].

These phenomena have an adverse effect on the performance of electronic devices, leading to the formation of emitter dips in the n–p–n bipolar transistors [8], the lowering of the breakdown voltage in p–n junctions [9] and the severe degradation of the life time in the surface region (dead layer) of silicon solar cells [10].

An alternative technique has been developed by our laboratory which involves doping the silicon through a polysilicon layer. This process has been reported to improve the performance and reduce the size of bipolar transistors [11]. In this paper the results of a detailed study carried out by X-ray topography and transmission electron microscopy on the lattice defects induced by the standard process and by the polysilicon technology are presented. The purpose of this comparison is to show the effect of each process on crystal imperfections.

2. Experimental procedure

Dislocation free (1 0 0) and (1 1 1) oriented, boron doped, CZ pulled, silicon wafers of resistivity nominally 1 Ω cm were used in these experiments.

Thin layers of polycrystalline silicon were grown on the specimens by chemical vapour deposition in a hot wall furnace at 600° C using a H_2 atmosphere containing 0.08 vol% SiH_4. The thicknesses of the films, ranging from 800 to 2000 Å, were carefully measured by Talystep as described elsewhere [12]. The phosphorus

*Work supported by C.N.R. Progetto Finalizzato Energetica.

 0022–2461/80/051124–07$02.70/0

predepositions were performed at 920, 1000 and 1100° C in a 0.27 vol% $POCl_3$ and 5.7 vol% O_2 atmosphere. The apparatus and the procedures have been described in a previous paper [6].

The reduction of the polycrystalline silicon film (PSF) thickness, due to the oxidation associated with the doping process, was deduced from measurements with Talystep of the thickness of the phosphorus glass (PSG) formed during the predepositions. Sheet resistivity determinations have been carried out by the four-point probe technique after the PSG has been removed in a dilute HF solution leaving the PSF.

The slices subjected to the predeposition processes have been observed using X-ray topography (XRT) and transmission electron microscopy (TEM).

3. Results

The predeposition experiments carried out at the three temperatures given above exhibited different rates of growth of the polysilicon grains as well as different types of crystallographic defects.

In this section a detailed description of the results obtained is given; reference is made only to the results from the specimens of (1 0 0) orientation, because the kinds of the induced defects in the (1 1 1) wafers were found to be the same, although some difference was noticed in the kinetics of their formation.

3.1. Phosphorus diffusion at 920° C

The grain size of the PSF was determined by TEM observations before and after the predeposition processes and an average value of about 500 Å was obtained in both cases.

In Fig. 1 an X-ray topograph of a wafer partially covered with a PSF of thickness about 800 Å, predeposited for 27 min, is shown. In the side corresponding to PSF no defect was revealed in the underlying single crystal. In the uncovered side dot-like defects, quite similar to those reported in a previous paper (see Fig. 1 in [13]), were evident. They were found to consist of aggregates of SiP precipitates. The TEM micrographs taken on the same specimen, shown in Fig. 2, clearly indicate the presence of randomly oriented particles confined within the PSF and having a length comparable with the average diameter of the grains. From the analysis of the electron diffraction patterns, it was confirmed that they are SiP precipitates having the same structure as detailed in [13]. After removing the PSF from the substrate, no defect was observed, in agreement with the X-ray observations.

This situation, which results in a higher sheet resistance for the PSF-covered side (point B in Fig. 3) than for the bare single crystal (point A in Fig. 3), is typical not only of this process, but is also found even for much longer times. In fact, it can be seen from Fig. 3 that, for a predeposition time of 90 min, the sheet resistance of a PSF-covered specimen, shown by point C, is lower than the value corresponding to the point A. Nevertheless the SiP precipitation still occurs, only within the PSF.

As a result of the oxidation associated to the predeposition, there is a reduction of the PSF thickness of 250 Å and 450 Å for 27 and 90 min, respectively. This implies that even a very thin PSF is sufficient to prevent the formation of lattice defects in the substrate.

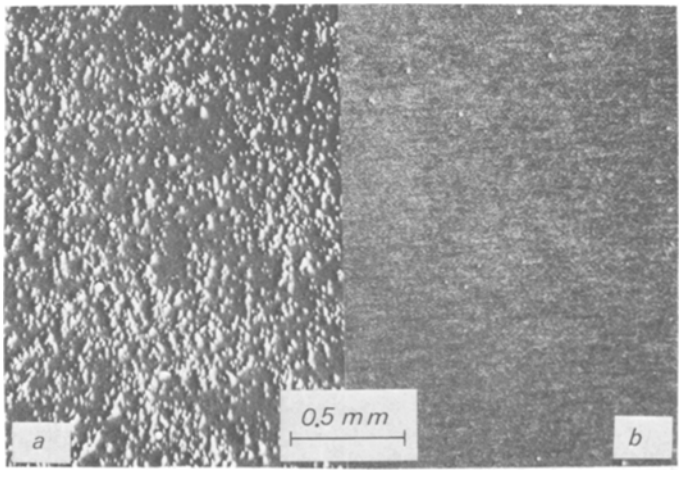

Figure 1 X-ray topographs of a wafer predeposited at 920° C for 27 min. (a) Uncovered side; (b) side covered with PSF.

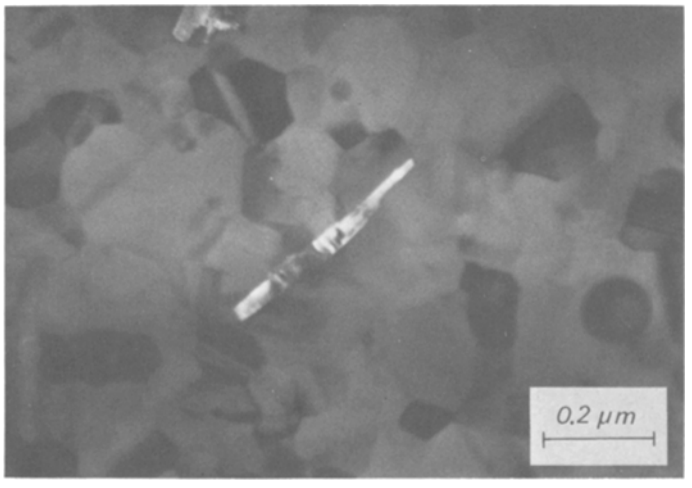

Figure 2 TEM micrograph of the specimen of Fig. 1b showing an SiP precipitate confined within the PSF. Dark-field image taken with a spot of the particle.

3.2. Phosphorus diffusion at 1000° C

The PSF used in these experiments was about 2000 Å thick; the average grain size was measured from both TEM micrographs and from the broadening of the X-ray diffraction peaks, and was found to be about 500 Å, as in the previous case. After the predepositions, TEM observations showed a marked increase in the grain size diameter, with values up to 3 μm (Fig. 4).

Fig. 5 refers to a Lang topograph taken on a wafer predeposited for 18 min. In the side of this figure corresponding to the bare silicon are present dislocation lines associated with the same dots, typical of SiP precipitation, observed at 920° C. From the contrast analysis of the dislocations, it was possible to conclude that they are aligned along the ⟨1 1 0⟩ directions parallel to the silicon surface and are of 60° type (Burgers vector $\mathbf{b} = (a/2)\langle 1\,1\,0\rangle$ inclined with respect to the surface). The growth mechanism of these dislocations is the same as that previously determined [4, 14], i.e. a climb motion due to absorption of silicon interstitials.

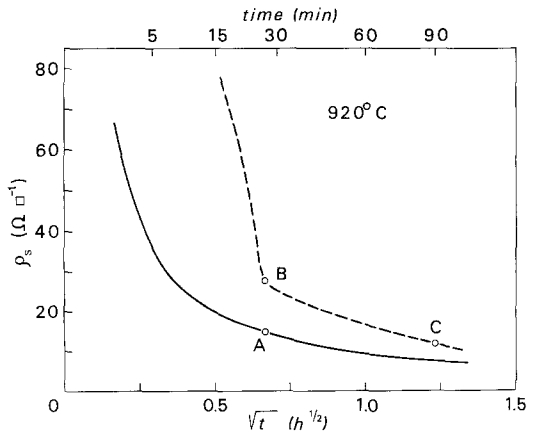

Figure 3 Sheet resistance against predeposition time for samples processed at 920° C. Solid curve: uncovered wafers; dashed curve: PSF-covered wafers. The determinations of ρ_s have been performed without removal of the PSF.

The side of Fig. 5 relative to the portion of the wafer covered with the PSF does not show the presence of such dislocations, although a residual contrast is observable, which is not characterizable by X-ray topography.

This region of the wafer was thinned for TEM observations after removal of the PSF; no defects were detected in the electron micrographs, probably due to the low density of such features.

By increasing the predeposition time, a linear growth of the climbing dislocations was noticed. By extrapolating to zero the dislocation length, a threshold time $t \simeq 11$ min (point T in Fig. 6) is obtained for their nucleation, which was confirmed by a series of X-ray topographs taken above and below this time. Two examples of such images corresponding to 18 and 41 min are reported in Fig. 6 band c. Defects of this type were never observed in the regions under the PSF, even for a 120 min predeposition time, which corresponds to a sheet resistance well below the value of the above mentioned threshold time ($\rho_s = 9\ \Omega\square^{-1}$*) (Fig. 6). Finally, the results obtained with a

*The normalized parameter called sheet resistivity $\rho_s(\Omega\square^{-1})$ is related to the resistivity ρ by $\rho_s = \rho/t = rW/L$ where r is the resistance, t is the thickness, W is the width and L is the length of the wafer.

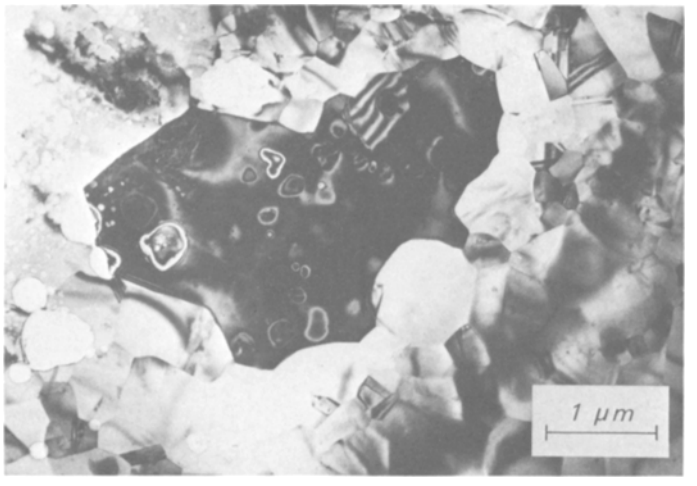

Figure 4 TEM micrograph showing the distribution of the grain size of the PSF after predeposition at 1000° C.

thinner PSF (about 1000 Å) were in qualitative agreement with those reported above.

3.3. Phosphorus diffusion at 1100° C

In this case the PSF used was again 2000 Å thick. For predeposition times as low as 5 min, an epitaxial regrowth of the PSF takes place, leaving behind a high density of heavily jogged dislocations as well as twins about 0.5 μm long, as shown by the TEM micrograph in Fig. 7. These defects are confined within the junction depth (about 1.3 μm) and are present for times up to 12 min, which was the longest time employed in these experiments. X-ray observations performed on specimens predeposited for 2 min did not reveal the presence of any defect in the single crystal underlying the PSF; however, the occurrence of climbing dislocations nucleated at damaged areas was noticed in the bare silicon side. Longer predeposition times (up to 12 min) led to the formation in the covered side of small linear defects, aligned along ⟨1 1 0⟩ directions parallel to the specimen surface, which were consistent with the twins observed in the TEM micrographs of Fig. 7. In agreement with the fast epitaxial regrowth, the sheet resistances of the two sides of the wafer were not markedly different and tended to coincide for times longer than 15 min.

Finally, it is found that the grain growth of the PSF is strongly affected by the doping process: annealing experiments carried out in N_2 atmosphere at this temperature did not result in a significant increase in the grain size.

4. Discussion

The experimental results indicate that the function of the PSF is twofold: (i) to provide preferential sites for the nucleation of SiP precipitates, (ii) to

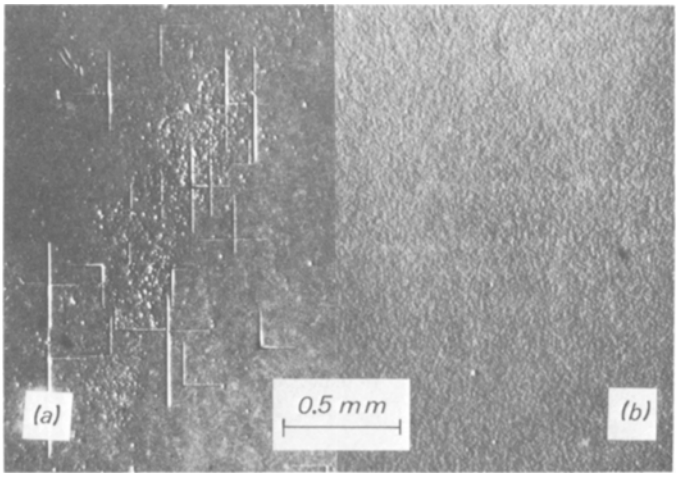

Figure 5 X-ray topograph taken on a wafer predeposited at 1000° C for 18 min. (a) Uncovered side; (b) side covered with PSF.

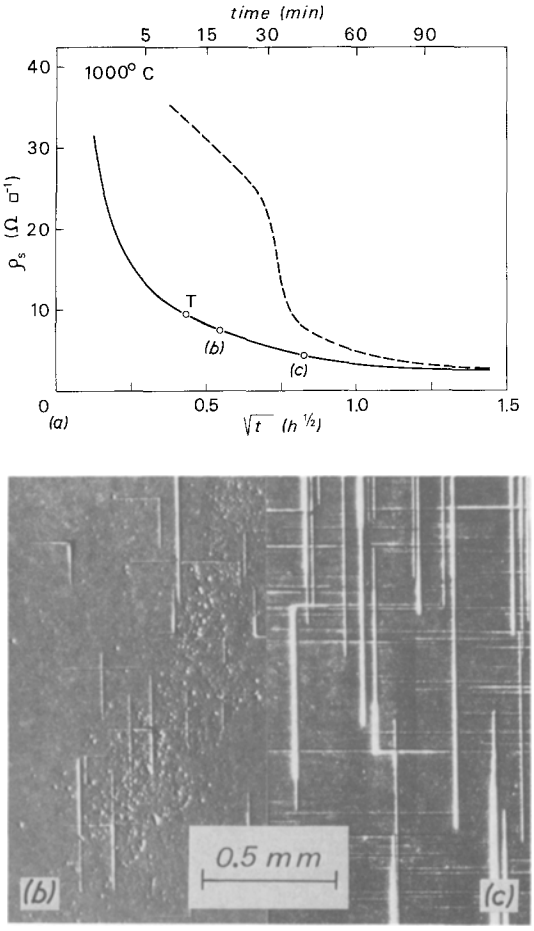

Figure 6 Sheet resistance against predeposition time for uncovered (solid curve) and PSF-covered (dashed curve) silicon wafers processed at 1000° C. (b) and (c) show X-ray topographs corresponding to 18 and 41 min doping times, corresponding to points (b) and (c) on the curve. The determinations of ρ_S have been performed without removal of the PSF.

absorb the excess of silicon interstitials, which, according to a previous work [4], is induced by the in-going phosphorus atoms.

The first statement is supported by the predepositions performed at 920° C. In fact, as long as the PSF is still present after the doping process, the precipitation is confined within it (Fig. 2) and no lattice defect was observed in the substrate (Fig. 1b).

As to the absorption of the excess of silicon interstitials, the experiments carried out at 1000° C show that it occurs within the PSF. In fact, in the underlying single crystal the presence of extrinsic stacking faults, which grow by climb of the bounding Frank partials during the doping process, was never detected [4]. In addition, neither the TEM nor the Lang (Fig. 5b) observations exhibit the formation of the 60° perfect dislocations, which take place as a result of an unfaulting reaction involving the stacking faults. Such dislocations are commonly observed in the bare silicon wafers, as reported in Fig. 5a and in [4].

Even at 1100° C the 60° climbing dislocations observable in the bare specimens are not present in the PSF covered wafers, where their formation might be expected because an epitaxial regrowth of the PSF takes place in the first minutes of the process. The excess interstitials are absorbed through negative climb by dislocations giving rise to the jobs observed in the micrograph of Fig. 7.

A further check of the ability of the PSF to absorb these interstitials, thus leaving a lower concentration of point defects in the underlying single crystal, is provided by the analysis of the doping profiles carried out in recent work [15], which show a marked reduction in the anomalous diffusion phenomena (i.e. high diffusivity tails and emitter dip effects in bipolar transistors).

Finally, with regard to the growth of the PSF grains, the present experimental work shows that it is strongly dependent on the doping process rather than on the temperature alone. In fact no variation in the grain size was detected after annealing at 1100° C in an inert ambient, whereas predeposition experiments performed at lower temperature (1000° C) resulted in a marked increase in the grain dimensions. Even this phenomenon may be attributed to the excess of silicon interstitials introduced by the in-going phosphorus atoms.

5. Summary and conclusions

In this paper it has been demonstrated that a predeposition process carried out through a polysilicon film has two distinct advantages. First, the precipitation of phosphorus is confined within the PSF, leaving the underlying single crystal free from this type of defect. Secondly, the PSF acts as a sink for the excess point defects induced by the in-going phosphorus, thus preventing the nucleation of both extrinsic stacking faults and dislocations.

An additional advantage of this technology is the possibility of also employing aluminium as a metal for ohmic contacts in very shallow junctions [16]. In fact, the presence of a PSF between the aluminium and the silicon single crystal produces

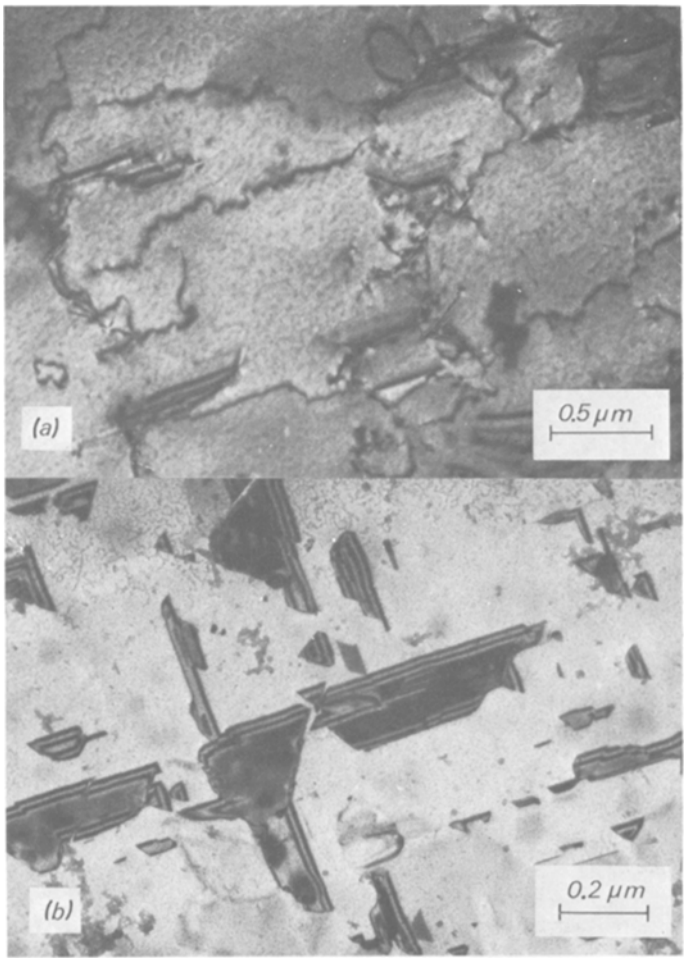

Figure 7 TEM micrograph taken on a PSF covered wafer, predeposited at 1100° C for 5 min, showing jogged dislocations and twins (a). The twins are in better contrast in (b), imaged in the (5 $\bar{1}$ 0) projection.

low contact resistances ($\rho_c < 10^{-4}\ \Omega\,cm^2$) even in absence of any subsequent thermal treatment. Moreover annealing cycles performed up to 400° C do not result in a junction deterioration.

This technology has been successfully employed in the fabrication of high efficiency silicon solar cells [17].

Acknowledgements

The authors are indebted to Mr P. Negrini and Mr G. Ruffini for their skilful technical assistance.

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Received 6 June and accepted 12 October 1979.